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(71)Applicant : SHARP CORP

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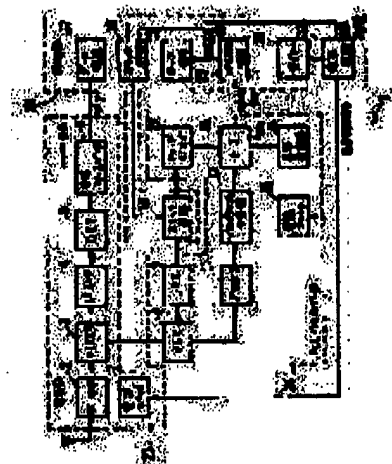
(72)Inventor : SUMIKAWA KEIICHIRO

(54) PHASE LOCKED LOOP CIRCUIT

(57)Abstract:

PURPOSE: To reduce the lock time at intermittent operation by providing a switching means and a voltage storage means storing an input voltage to a voltage controlled oscillator circuit just before the open circuit between a phase comparator and an LPF.

CONSTITUTION: The switching circuit 16 interposed between the phase comparator (PD) 13 and the LPF 9, a charge pump 10 storing an input voltage to the voltage controlled oscillator circuit (VCO) 8 just before the open circuit and a switch control means 18 opening a loop by the switch 16 in the presence of the open circuit command, giving the said storage voltage to the VCO 8 when the open command exists and closing the loop by the switch 16 when the phase difference detected by the PD 13 reaches a prescribed value or below, are provided. When the power of the PLL circuit is switched from OFF to ON in the intermittent operation, the preceding frequency is taken over. Moreover, the loop is closed with a large phase difference and the frequency is not largely deviated. The lock time at the intermittent operation is shortened by the operation.



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H 04 B 1/20 U-7251-5K
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⑪ 発明の名称 フェーズ・ロックド・ループ回路
⑫ 特 許 昭62-193460
⑬ 出 願 昭62(1987)8月7日
⑭ 発 明 者 澤 川 恵 一 郎 大阪府大阪市阿倍野区長池町22番22号 シヤープ株式会社
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⑯ 代 理 人 弁護士 本庄 実男

明 細 書

1. 発 明 の 名 称

フェーズ・ロックド・ループ回路

2. 発 明 の 要 求 の 範 囲

1. 位相比較回路と、ローパスフィルタと、電圧制御回路とがループを形成してなるフェーズ・ロックド・ループ回路において、

位相比較回路とローパスフィルタの間またはローパスフィルタと電圧制御回路の間に介在されてループをオープンする手段と、オープン直前の電圧制御回路からの入力電圧を記憶する電圧記憶手段と、オープン後がある一定時間経過後にループをオープンすると共にリセット手段がある一定時間経過後に前記記憶電圧を前記電圧制御回路に出力し前記位相比較回路で位相差を検出し位相差が所定値以下となったときに前記スイッチ手段でループをクローズするスイッチ制御手段とを具備したことを特徴とするフェーズ・ロックド・ループ回路。

3. 発 明 の 好 好 施 施 例

(構成上の所属分野)

本発明は、フェーズ・ロックド・ループ回路に關し、更に詳しくは、周知動作をさせる場合に周知信号を伝送回路を通過できるようにしたフェーズ・ロックド・ループ回路に關する。

(従来の技術)

コードレス電話やページャ等の無線局間通信においては、電波の増幅を助ぐために、受信すべき電波の増幅があるまでは周知動作を行なっている。

即ち、受信側素子体に電力を供給して電波を受信できる状態で待機する待ち受け動作と、受信側素子の部分以外に電力の供給をカットして電波を受信できないが電力消費を抑制する停止動作とを交互に繰り返すことを行なっている。

フェーズ・ロックド・ループ回路(以下、FLL回路という)は、周知用増幅機のチューナ部のシンセサイザーとして広く使用されており、上記周知動作時には、FLL回路も周知動作をさせるれている。

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(図解が特許しようす 図解風)

チャージ部にP.L.L.回路を用いた場合、P.L.L.回路の周波数引き込み増幅(プラインレンジ)を経てロックされるまでの時間(ロックタイム)は正しい発振状態に入れない。従って、ロックタイムは短い方が好ましい。

ところが、P.L.L.回路を周波数引き込み増幅と、その増幅電圧オフから出る上があるため、周波数引き込みロックタイムが長くなってしまい好ましくない。

従って、本発明の目的とするところは、周波数引き込み増幅におけるロックタイムを短縮可能なP.L.L.回路を提供することにある。

(問題点を解決するための手段)

本発明のP.L.L.回路は、位相比較回路と、ローパスフィルタと、電圧制御回路とがループを形成して成るフェーズ・ロックド・ループ回路において、位相比較回路とローパスフィルタの間またはローパスフィルタと電圧制御回路の間に接続されてループをオープンする手段と、オープン状態の電圧制御回路と位相比較回路への入力電圧を制御する電

圧制御手段と、オープン指令があると前記スイッチ手段でループをオープンすると共に、ローパスフィルタと電圧制御回路とを前記電圧制御回路の出力に接続し、位相比較回路の出力で位相比較回路の出力を制御し、位相比較回路の出力が所定値以下となったときに前記スイッチ手段でループをクローズするスイッチ制御手段とを具備したことを特徴とするものである。

(作用)

本発明のP.L.L.回路では、電圧制御手段によって電圧制御回路の出力に接続して、位相比較回路の出力が所定値以下となったときにループをクローズすることが出来るので、周波数引き込み増幅において、P.L.L.回路の電圧がオフからオンに切り替わった時、位相比較回路からスタートできる。従って、位相比較回路の出力が所定値以下となったときにループをクローズすることが出来るので、位相比較回路が所定値以下となったときにループをクローズして、周波数引き込み増幅を大きく外してしまうことが防止される。

そこで、これらの作用より、周波数引き込み増幅

のロックタイムを短縮することが出来る。

そして、周波数引き込み増幅で周波数引き込み増幅の出力電圧をロックタイムの短縮によって短縮することが出来るようになるから、周波数引き込み増幅の出力電圧を短縮出来るようになる。

(実施例)

以下、図に示す実施例に基づいて本発明を更に詳しく説明する。ここに示す図は本発明の一実施例のP.L.L.回路を含む周波数引き込み増幅のブロック図、第1図は本発明におけるスイッチ手段と電圧制御手段とを対応する回路部分の具体的な構成、第2図は本発明におけるスイッチ制御手段と電圧制御手段との具体的な構成、第3図は第1図に示す周波数引き込み増幅の具体的な構成である。尚、図に示す実施例により本発明が限定されるものでない。

第1図に示す周波数引き込み増幅1は、発振部2と、P.L.L.回路3と、周波数引き込み増幅4とを有する。P.L.L.回路3は、位相比較回路5と、ローパスフィルタ6と、電圧制御回路7とを有する。

発振部2は、従来の周波数引き込み増幅であり、周波数引き込み増幅のための電圧制御回路7が接続され

ている。

P.L.L.回路3は、位相比較回路5と、ローパスフィルタ6と、電圧制御回路7とを有する。P.L.L.回路3は、位相比較回路5と、ローパスフィルタ6と、電圧制御回路7とを有する。P.L.L.回路3は、位相比較回路5と、ローパスフィルタ6と、電圧制御回路7とを有する。P.L.L.回路3は、位相比較回路5と、ローパスフィルタ6と、電圧制御回路7とを有する。

ここで注意すべきことは、ローパスフィルタ6と電圧制御回路7との間に、スイッチ回路8が介在されていることである。

位相比較回路5は、チャージポンプ10への出力の他に、位相比較回路5の出力が出力するアンロック信号を出力している。

第2図は、ローパスフィルタ6、スイッチ回路8、チャージポンプ10を具体的に構成したものである。

制御部9は、前記スイッチ回路8を制御するためのスイッチ制御回路11と、周波数引き込み増幅4のためのタイマー回路12および電圧制御回路13と、前記位相比較回路5からのアンロック

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の信号に応じて制御部を動作させるパルス信号は、図2の図20と等価している。位置検出信号は、前記スイッチ制御回路19に入力されている。

第3図は、スイッチ制御回路19、パルス検出回路20を具体的に示したものである。

次に、図1の図10及び図11に示す信号処理部を参照し、動作時の動作を説明する。

まず、待ち受け動作の状態では、受信部21、アンプ・コンパライザ部24、制御部25の全てに電力が供給され、電圧を感知できる状態で待機している。ここで制御部25は、送信用の周波数の送信チャンネルと、受信用の周波数の受信チャンネルを有しているが、待ち受け動作では、送信チャンネルの電圧を待っている。

待ち受け動作を所定時間継続すると、タイマー回路21及び電圧制御回路24から出力される電圧信号が「H」になる。すると、第3図に示すようにスイッチ回路19がオフされ、第2図に示すようにローパスフィルタ23のコンデンサCは定電圧の電圧を保持した状態となる。

する間継続となり、それ以外の待ち受け動作における周波数とほぼ等しい周波数である。従って、立ち上がりに関する時間が短縮される。

ところで、受信部21から入力される電圧制御部25からの信号と基準電圧21からの信号の電圧差が大きいと、両信号の周波数が合致していても、ループがクローズされた時に周波数が大きく外れてしまう危険がある。

しかし、スイッチ回路19は、位置検出信号を待ってかち同じられるため、かかる周波数はずれは抑えられる。即ち、第3図に示す「H」状態によって、電圧立ち上がり時にはスイッチ回路19が閉じないようとする。そして、電圧差が大きい時に出力されるアンプ・コンパライザ部24からの信号は、スイッチ回路19を閉じないようとする。そして、電圧が完全に立ち上がり、且つ、電圧差が小さくなってアンプ・コンパライザ部24からの信号が出力されない時は、スイッチ回路19が閉じられる。

そこで結局、周波数が定合致し、且つ、電圧差のない状態でループがクローズされるので、周

波数 21は、スイッチ回路19をオフにした後、電圧スイッチ回路19及び19を動作し、受信部21とアンプ・コンパライザ部24の電圧を遮断する。また、制御部25のデータ記憶回路17、ロック検出回路18、パルス検出回路20の電圧を遮断する。かくして、電圧の受給は出来ないが、消費電力を抑制した停止動作に移行する。

停止動作を所定時間継続すると、タイマー回路21及び電圧制御回路24は、電圧信号を「H」にし、受信部21及びアンプ・コンパライザ部24の電圧をオンとする。また、制御部25のデータ記憶回路17、ロック検出回路18、パルス検出回路20の電圧をオンにする。

しかし、スイッチ回路19は、電圧信号が「H」になっても、パルス検出回路20からの位置検出信号が入力されない限り、ループをクローズにしない。

そこで、電圧制御回路24の制御の周波数は、ローパスフィルタ23に保持されていた電圧に比例

動作外れを防止し、短時間でアンプ・コンパライザ部24を動作する。

かくして、アンプ・コンパライザ部24を動作させるため、待ち受け動作の時間を短縮できることになる。そこで、受信すべき電圧の電圧があるまでの時間に「待ち受け時間」が消費する電力を低減できることとなる。

【発明の効果】

本発明によれば、位置検出信号と、ローパスフィルタと、電圧制御回路24とがループを形成してあるフェーズ・ロック・ループ回路において、位置検出信号とローパスフィルタの間またはローパスフィルタと電圧制御回路24の間に接続されてループをオープンする手段と、オープン直後の電圧制御回路24への入力電圧を記憶する電圧記憶手段と、オープン指令があると前記スイッチ手段でループをオープンすると共にクローズ指令があると前記電圧記憶手段を電圧記憶手段から出力し電圧記憶手段が記憶した電圧を記憶手段に保持した状態で前記スイッチ手段でループ

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をクロージングスイッチ制御手段を含むとしたこととを特徴とするフェーズ・ロッキング・ループ回路が提供され、これにより周波数利を効率的に使用する時間すなわちロッキングタイムを短縮できるようになる。

そこで、かかるフェーズ・ロッキング・ループ回路を用いた換気扇制御装置において、周波数利を効率的に使用する時間すなわちロッキングタイムを短縮できることとなり、低消費電力化を促進できる。

図面を参照して説明する。

第1図は本発明の一実施例のFLL回路を含む換気扇制御装置のブロック図、第2図は本発明におけるスイッチ手段と周波数利手段とに相当する回路部分の具体的な例、第3図は本発明におけるスイッチ制御手段に相当する回路部分の具体的な例、第4図は第1図に示す回路図の各部の信号波形図である。

【符号の説明】

1…換気扇制御装置

- 2…電圧制御回路
- 3…ローパスフィルタ
- 4…チャージポンプ
- 5…位相比較回路
- 6…スイッチ回路
- 7…スイッチ制御回路
- 8…パルス幅変換回路
- 9…タイマー回路
- 10…電圧制御回路
- 11…電圧スイッチ回路

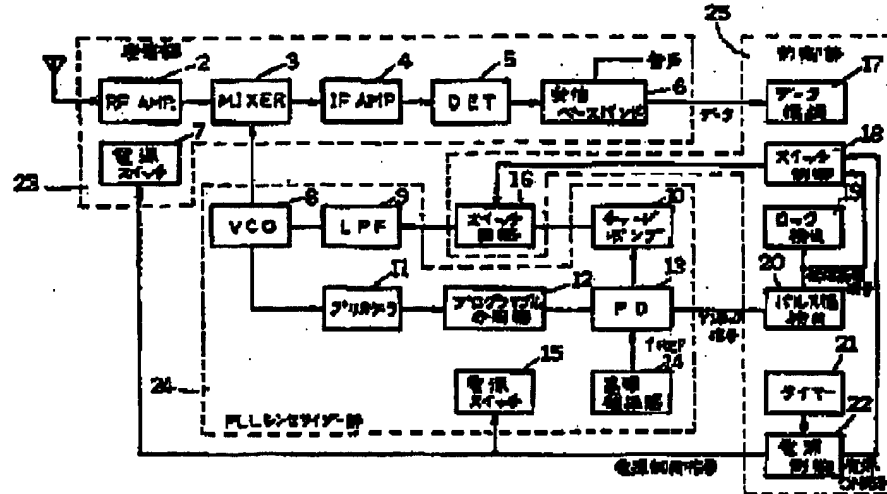
出願人 シャープ株式会社
代理人 弁護士 中野 実男

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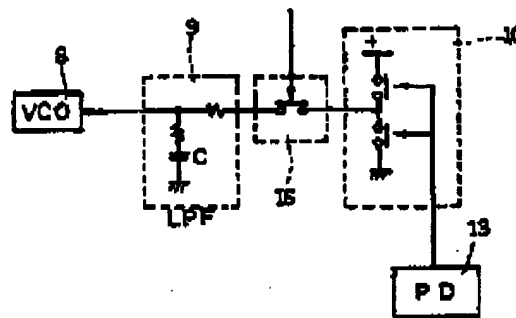
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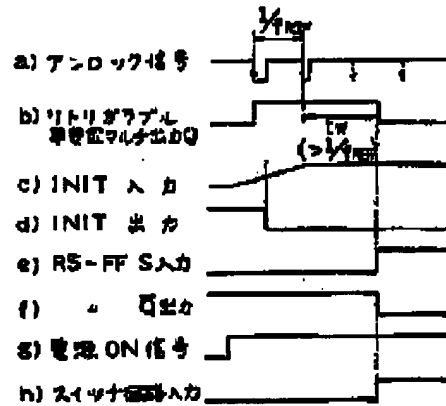
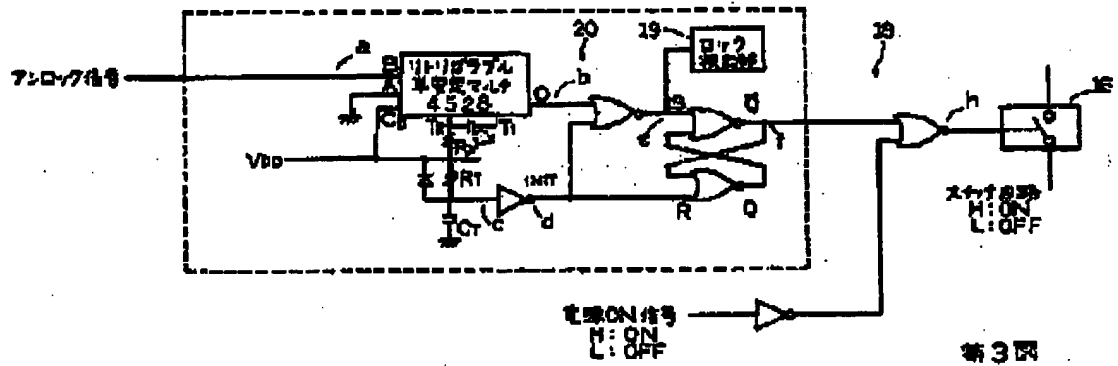
第1図



第2図



特開 2003-41526 (6)



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(71)Applicant : NEC CORP

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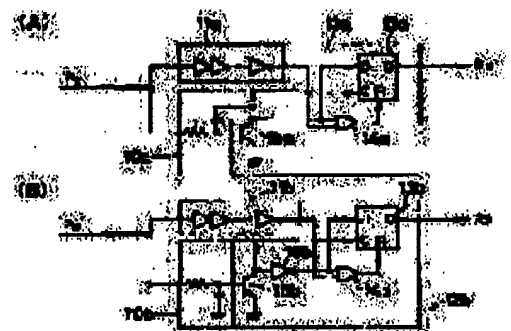
(72)Inventor : JOKURA ATSUSHI

(54) PLL CIRCUIT

(57)Abstract:

PURPOSE: To improve S/N of the PLL circuit in the frequency synthesizer of a reception system by providing a dead zone for phase comparison and realizing stable synchronous convergence.

CONSTITUTION: A phase leading PD pulse is delayed by a delay device 11b and is inputted to the clock input of a D-FF 13b. The PD pulse is integrated by a time constant circuit 10b, and this integral waveform is compared with the threshold of a transistor TR 15b, and a pulse is generated when it is larger than this threshold. This pulse is inputted to the data input of the D-FF 13b to latch the PD pulse, and the D-FF 13b is reset by an OR gate 14b at the time of disappearance of the PD pulse. Its Q output RD is supplied to a charge pump and a loop filter to obtain the control voltage of a VCO. Consequently, the dead zone is determined by OR of the time constant circuit 10b and the threshold of the TR 15b, and the PD pulse larger than the dead zone is outputted as it is, and therefore, synchronous convergence is stabilized.



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CLAIMS

[Claim(s)]

[Claim 1] An armature-voltage control oscillation means and a phase-comparison means to make the phase comparison of this oscillation output frequency signal and external oscillation signalling frequency, It is a PLL circuit including a control-voltage generation means to generate the control voltage of the aforementioned armature-voltage control oscillation means according to this phase-comparison output. the aforementioned control-voltage generation means A delay means by which the aforementioned phase-comparison output is delayed, and the time constant circuit which considers the aforementioned phase-comparison output as an input, The PLL circuit characterized by being constituted including a latch means to cancel this latch state when the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears by the output of the aforementioned delay means so that the aforementioned control voltage may be generated using this latch output.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] Especially this invention relates to the PLL circuit used in order to obtain the stable synchronizing signal in strange recovery technology about a PLL (phase locked loop) circuit.

[0002]

[Description of the Prior Art] A PLL circuit detects the phase contrast of the reference frequency signal given from the outside, and the dividing output which carried out dividing of the oscillation output of VCO (voltage controlled oscillator), controls VCO by direct current voltage according to the phase contrast, and obtains a stable oscillation output.

[0003] In the receiving system, it mixed with the receiving RF signal by having made this oscillation output into the local oscillation signal, and the IF signal was created and alignment has been obtained for the frequency change at the time of a channel change by changing the division ratio of a counting-down circuit (program divider), or using a direct digital synthesizer etc. and changing the reference frequency signal itself to the source of a signal.

[0004] In local oscillation frequency synthesizer SASHIZA, for a high-speed frequency change, the high interest profit design of a system is performed, but on the other hand noise bandwidth becomes large, it is easy to incorporate noise in a system, and C/N-ary of an oscillation output pose a problem. The method of extending the neutral zone (DETTO zone) in a phase comparison as a negative measure in such a case is taken.

[0005] Drawing 5 is the circuit diagram showing the portion of the phase comparator of the conventional PLL circuit shown in JP,63-260317, A. reference frequency signal fR with which the 1st D-FF and 23 were impressed to the 2nd D-FF, and 24 was impressed [21] to the clocked-into terminal of 1st D-FF22 for a charge pump and 22 The 1st delayed delay circuit and dividing signal fP with which 25 was impressed to the clocked-into terminal of 2nd D-FF23 It is the 2nd delayed delay circuit. 25 and 24 are delay circuits and 28 and 29 are the DETTO zone expansion signal DZ. It is the circuit which responds and chooses the amount of delay.

[0006] Next, operation is explained. input terminal D1 of D-FF22 **** -- reversal output Q2 of D-FF it impresses -- having -- input terminal D2 of D-FF23 **** -- reversal output Q1 of D-FF22 it impresses -- having -- output Q1 it is impressed by the gate of NMOS26 of the charge pump circuit 21 -- having -- output Q2 It is impressed by the gate of NMOS27.

[0007] DETTO zone expansion signal DZ If it turns OFF ("0"), the delay signal of the last stage of a delay circuit will be chosen from selection circuitries 28 and 29.

[0008] First, dividing signal fP It receives and is the reference frequency signal fR. It is fP, as it is shown in drawing 6 (A), when the phase is in agreement. fR By the standup, both D-FF 22 and 23 incorporate a mutual reversal output "1", and it is an output Q1 respectively. And Q2 It outputs. These outputs Q1 and Q2 It goes up by the inclination shown as a solid line like drawing 6 (C), and is threshold voltage Vt. It is TD the time of reaching. Output R1 of selection circuitries 28 and 29 R2 It starts.

[0009] That is, the amount of the maximum delay of delay circuits 24 and 25 is TD. It has designed so that it may become equal, and it is an output R1 and R2. It is reset and both D-FF 22 and 23 are outputs Q1 and Q2. It falls, therefore neither of NMOSes 26 and 27 turn on in this case, and the output PD according to phase contrast is not outputted.

[0010] As shown by drawing 6 (B), after fR ' has become early for 10ns, D-FF22 incorporates "1" and is an output Q1. It starts like dotted-line ** of (C). It is behind for 10ns and D-FF23 is fP. "1" is incorporated in a standup and it is the output Q2. It goes up. Next, when R1 ' is outputted from a selection circuitry 28, it is reset and D-FF23 is an output Q2. Vt Before reaching, it falls like dashed line ** of (C).

[0011] On the other hand, it is the output Q1 of D-FF22. Vt It reaches and is the output R2 of a selection circuitry 29. D-FF22 will be reset. Therefore, output Q1 Vt The period which became above, and NMOS26 are turned on, and the output PD according to phase contrast "0" is outputted. That is, in the case of drawing 6 (C), it is fR. When it becomes early, it is an output R2. Before being outputted, it is surely Vt. Reaching, a dead zone serves as zero.

[0012] Next, DZ= "1" is a case and, as for drawing 6 (D), the delay signal with few amounts of delay than the time of DZ=

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"0" is chosen. It is fR first. fP When the phase is in agreement, it is t
is TD. Since it becomes early, it is Q1. Q2 Vt D-FF 22 and 23 is reset without reaching.

[0013] Now and output R1 R2 TD It is fR when it is a delay signal early for 10ns. When it becomes early for 10ns like drawing 6 (D), it is the output Q1 of D-FF22. It goes up, as shown by the solid line of (D), and it is Vt. Since an output R2 occurs just before reaching, D-FF22 is reset, and it is Q1. It falls.

[0014] Therefore, in the case of drawing 6 (E), it is fR. fP Phase contrast is an output Q1 within in 10ns. Vt Output PD corresponding to [before reaching D-FF22 will surely be reset and NMOS26 is turned on, and] phase contrast It is not generated. That is, the dead zone for 10ns is prepared. the same -- fP if it comes out 10 or less ns when it becomes earlier than fR -- output Q2 of D-FF23 Vt Since D-FF23 is reset before reaching, the dead zone for 10ns occurs.

[0015] By preparing a dead zone, frequent generating of a control pulse which serves as disturbance of VCO in the state where the PLL circuit locks was prevented, and noise signals, such as a jitter nozzle, were also omitted, and S/N is improved sharply.

[0016]

[Problem(s) to be Solved by the Invention] In the PLL circuit constituted from a conventional phase-comparison circuit mentioned above, there is a problem on which the reaction of a system becomes slow to the phase contrast near the dead zone.

[0017] For example, fR fP When the case where received and it becomes early for 12ns is assumed, it comes to be shown in drawing 7 . In the state of the dead zone 0 of DZ = "0", it is an output Q1. Vt It can put at about 12ns and the time it is over is PD. Although "1" is outputted for 12ns as a signal a dead-zone 10ns [of DZ = "1"] state -- output Q1 Vt about 2ns of time to exceed -- becoming -- PD As a signal, for 2ns continues but the rate of the integration voltage value change which controls VCO which lets a loop filter pass boils "1" dully.

[0018] If the property of this phase comparison is shown in drawing, it will become like drawing 8 . fR fP Since the time which sees relatively and is deleted in 10ns for the dead-zone setup becomes small when phase contrast is large, although influence decreases, the sensitivity as a remarkable system deteriorates near the dead zone.

[0019] Specifically, although it is convenient to change to near shift frequency at the time of the change of the oscillation frequency of a PLL circuit, alignment near a convergence value is affected and there is a trouble which the phenomenon in which vibration drags on to a convergence value tends to produce.

[0020] The purpose of this invention is offering the PLL circuit which enabled stable synchronous convergence, preparing a dead zone at the time of a phase comparison.

[0021]

[Means for Solving the Problem] A phase-comparison means to make the phase comparison of an armature-voltage control oscillation means, and this oscillation output frequency signal and external oscillation signalling frequency according to this invention, It is a PLL circuit including a control-voltage generation means to generate the control voltage of the aforementioned armature-voltage control oscillation means according to this phase-comparison output. the aforementioned control-voltage generation means A delay means by which the aforementioned phase-comparison output is delayed, and the time constant circuit which considers the aforementioned phase-comparison output as an input, When the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears by the output of the aforementioned delay means, the PLL circuit characterized by being constituted including a latch means to cancel this latch state so that the aforementioned control voltage may be generated using this latch output is obtained.

[0022]

[Example] It explains in detail, referring to a drawing about the example of this invention below.

[0023] Drawing 1 is the block diagram of the example of this invention, and is reference frequency fR. The output of generated VCO 1 turns into one input of a phase comparator 3. Frequency fP which carried out dividing of the oscillation frequency of VCO7 to the other inputs of this phase comparator 3 with the counting-down circuit 2 The signal is impressed.

[0024] It is the lead signal PD of the pulse width according to the phase contrast from a phase comparator 3. It is behind, Signal PU is outputted and it is inputted into filter circuits 4a and 4b, respectively. These filter circuits 4a and 4b are circuits of the feature portion of this invention, and the one example is shown in drawing 2 . They are PD and PU, a dead zone being set up in these filter circuits 4a and 4b. Phase contrast signals RU and RD with which pulse width (phase contrast information is included) does not change It is generated.

[0025] These phase contrast signals RU and RD It becomes the control voltage of VCO7 by being inputted into a loop filter 6 and finding the integral through the charge pump 5.

[0026] The output of this VCO7 serves as local oscillation frequency in a receiving system, change instructions of a receiving channel are answered, the oscillation frequency fR of reference frequency VCO 1 and the division ratio of the program divider 2 are controlled, and the PLL frequency synthesizer is constituted.

[0027] Drawing 2 (A) and (B) are each example circuit diagram of the filter circuits 4a and 4b of drawing 1 . First, if

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drawing 2 (A) is referred to, it is the lead signal PU. It is inputted into respectively. The delay output of delay circuit 11a turns into a clocked into of D-FF13a which constitutes latch circuit 12a. [0028] The output of time constant circuit 10a turns into a base input of PNP transistor 15a which constitutes latch circuit 12a, and the emitter output of this transistor 15a turns into one input of OR-gate 14a while turning into a data input of D-FF13a. The delay output of delay circuit 11a is impressed to the other inputs of this OR-gate 14a, or the output is the reset input of D-FF13a. And the reversal Q output of D-FF13a is RU. It becomes.

[0029] Drawing 2 (B) is the delay signal PD. Although it consists of delay circuit 11b, time constant circuit 10b, and latch circuit 12b concretely also about the side The polarity of the power supply line of time constant circuit 10b and the polarity of transistor 15b in a latch circuit progress, and it is Signal PU. It has become contrary to a side. Moreover, the collector output of transistor 15b is inverted in inverter 16b, and is the data input of D-FF13b, and one input of OR-gate 14b.

[0030] Drawing 3 is each signal wave form view showing operation of the circuit of drawing 2 (B), and is fR. fP When it receives and a phase is overdue, it is the delay signal PD. Two PDs from which it is a thing at the time of being outputted, and it is behind in this example, and a degree differs The pulse is shown.

[0031] PD shown in (C) A pulse is changed into the loose wave (integration wave) of the standup shown in (d) with the time constant of time constant circuit 10b. This wave is the threshold V_t of transistor 15b. PD which is not attained By the pulse, transistor 15b does not turn on and, therefore, the data input signal (D input signal) from inverter 16b to D-FF13b is not generated. On the other hand, an integration wave is Threshold V_t . PD to attain By the pulse, transistor 15b is generated, as it turns on and a data input signal shows (e) from inverter 16b, and for this data input signal, an integration wave is Threshold V_t . It is generated until it becomes smallness.

[0032] the clocked into of D-FF13b -- PD a pulse -- time t_D only -- **** delay PD shown in delayed (f) The pulse is supplied. Here, it is a time delay t_D . Same [in the time t_M (refer to drawing (e)) to become settled with the time constant of time constant circuit 10b / almost] or it is t_M . t_D If it selects to smallness a little, it synchronizes with the standup timin timing of a clock signal (delay pulse PD), and a data input signal is incorporated and latched to D-FF13b.

[0033] Delay PD It is the filter circuit output RD which a latch state is reset and is shown in (g) as a result since D-FF13b will be reset by the output of OR-gate 14b, if a pulse falls. It will be obtained.

[0034] Therefore, lead signal PD according to phase contrast Therefore, it is the threshold V_t of filter circuit 12b, without being inputted into the latter charge pump 5 by letting filter circuit 4b (drawing 1) pass depending on the degree of the phase contrast. Time t_M to become settled It becomes a dead zone.

[0035] phase-lead-lag-network signal PD exceeding a dead zone ***** -- without the wave of the pulse changing, since there is no bird clapper dully like the former comparatively, the thing of the integration [by which it is outputted to the charge pump 5] voltage value change which controls [near the dead zone / come out and] VCO7 shown in drawing 4 as a phase-comparison property is obtained.

[0036] In addition, outputs RU and RD of filter circuits 4a and 4b PU and PD Receiving time delay TD If it attaches, it is a dead zone t_M . It can compare and ignore at the convergence time (order for 1 or less ms) demanded also as 100ns (10MHZ) or more than it at the time of the channel change of local oscillation frequency.

[0037] Stopping at the circuit of drawing 2 only being shown in an example, it is clear for various circuit deformation to be possible.

[0038]

[Effect of the Invention] There is an effect that a highly efficient PLL circuit without vibration near the convergence value or a tailing phenomenon is realizable, at the time of a channel change, setting up the dead zone in a phase comparison, when PLL is designed by high interest profit for the high-speed channel change which was described above and which is demanded in a PLL receiving system like according to this invention.

[0039] If it states quantitatively, there is an improvement of 10dB or more with an S/N value, and shortening for 2ms or more can be aimed at in channel change convergence time.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the PLL circuit used in order to obtain the stable synchronizing signal in strange recovery technology about a PLL (phase locked loop) circuit.

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PRIOR ART

[Description of the Prior Art] A PLL circuit detects the phase contrast of the reference frequency signal given from the outside, and the dividing output which carried out dividing of the oscillation output of VCO (voltage controlled oscillator), controls VCO by direct current voltage according to the phase contrast, and obtains a stable oscillation output.

[0003] In the receiving system, it mixed with the receiving RF signal by having made this oscillation output into the local oscillation signal, and the IF signal was created and alignment has been obtained for the frequency change at the time of a channel change by changing the division ratio of a counting-down circuit (program divider), or using a direct digital synthesizer etc. and changing the reference frequency signal itself to the source of a signal.

[0004] In local oscillation frequency synthesizer SASHIZA, for a high-speed frequency change, the high interest profit design of a system is performed, but on the other hand noise bandwidth becomes large, it is easy to incorporate noise in a system, and C/N-ary of an oscillation output pose a problem. The method of extending the neutral zone (DETTO zone) in a phase comparison as a negative measure in such a case is taken.

[0005] For a charge pump and 22, 21 is the reference frequency signal fR with which drawing 5 was the circuit diagram showing the portion of the phase comparator of the conventional PLL circuit shown in JP,63-260317,A, the 1st D-FF and 23 were impressed to the 2nd D-FF, and 24 was impressed to the clocked-into terminal of 1st D-FF22. 25 is the 1st delayed delay circuit and the dividing signal fP impressed to the clocked-into terminal of 2nd D-FF23. It is the 2nd delayed delay circuit. 25 and 24 are delay circuits and 28 and 29 are the DETTO zone expansion signal DZ. It is the circuit which responds and chooses the amount of delay.

[0006] Next, operation is explained. input terminal D1 of D-FF22 **** -- reversal output Q2 of D-FF it impresses -- having -- input terminal D2 of D-FF23 **** -- reversal output Q1 of D-FF22 it impresses -- having -- output Q1 it is impressed by the gate of NMOS26 of the charge pump circuit 21 -- having -- output Q2 It is impressed by the gate of NMOS27.

[0007] DETTO zone expansion signal DZ If it turns OFF ("0"), the delay signal of the last stage of a delay circuit will be chosen from selection circuitries 28 and 29.

[0008] First, dividing signal fP It receives and is the reference frequency signal fR. It is fP, as it is shown in drawing 6 (A), when the phase is in agreement. fR By the standup, both D-FF 22 and 23 incorporate a mutual reversal output "1", and it is an output Q1 respectively. And Q2 It outputs. These outputs Q1 and Q2 It goes up by the inclination shown as a solid line like drawing 6 (C), and is threshold voltage Vt. It is TD the time of reaching. Output R1 of selection circuitries 28 and 29 R2 It starts.

[0009] That is, the amount of the maximum delay of delay circuits 24 and 25 is TD. It has designed so that it may become equal, and it is an output R1 and R2. It is reset and both D-FF 22 and 23 are outputs Q1 and Q2. It falls, therefore neither of NMOSes 26 and 27 turn on in this case, and the output PD according to phase contrast is not outputted.

[0010] As shown by drawing 6 (B), after fR ' has become early for 10ns, D-FF22 incorporates "1" and is an output Q1. It starts like dotted-line ** of (C). It is behind for 10ns and D-FF23 is fP. "1" is incorporated in a standup and it is the output Q2. It goes up. Next, when R1 ' is outputted from a selection circuitry 28, it is reset and D-FF23 is an output Q2. Vt Before reaching, it falls like dashed line ** of (C).

[0011] On the other hand, it is the output Q1 of D-FF22. Vt It reaches and is the output R2 of a selection circuitry 29. D-FF22 will be reset. Therefore, output Q1 Vt The period which became above, and NMOS26 are turned on, and the output PD according to phase contrast "0" is outputted. That is, in the case of drawing 6 (C), it is fR. When it becomes early, it is an output R2. Before being outputted, it is surely Vt. Reaching, a dead zone serves as zero.

[0012] Next, DZ= "1" is a case and, as for drawing 6 (D), the delay signal with few amounts of delay than the time of DZ= "0" is chosen. It is f R first. fP When the phase is in agreement, it is the output R1 of a delay circuit. R2 What is generated is TD. Since it becomes early, it is Q1. Q2 Vt D-FF 22 and 23 is reset without reaching.

[0013] Now and output R1 R2 TD It is fR when it is a delay signal early for 10ns. When it becomes early for 10ns like drawing 6 (D), it is the output Q1 of D-FF22. It goes up, as shown by the solid line of (D), and it is Vt. Since an output R2 occurs just before reaching, D-FF22 is reset, and it is Q1. It falls.

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[0014] Therefore, in the case of drawing 6 (E), it is fR. fP Phase contr
corresponding to [before reaching D-FF22 will surely be reset and NMOS26 is turned on, and] phase contrast It is not
generated. That is, the dead zone for 10ns is prepared. the same - fP if it comes out 10 or less ns when it becomes earlier
than fR - output Q2 of D-FF23 Vt Since D-FF23 is reset before reaching, the dead zone for 10ns occurs.
[0015] By preparing a dead zone, frequent generating of a control pulse which serves as disturbance of VCO in the state
where the PLL circuit locks was prevented, and noise signals, such as a jitter nozzle, were also omitted, and S/N is
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EFFECT OF THE INVENTION

[Effect of the Invention] There is an effect that a highly efficient PLL circuit without vibration near the convergence value or a tailing phenomenon is realizable, at the time of a channel change, setting up the dead zone in a phase comparison, when PLL is designed by high interest profit for the high-speed channel change which was described above and which is demanded in a PLL receiving system like according to this invention.

[0039] If it states quantitatively, there is an improvement of 10dB or more with an S/N value, and shortening for 2ms or more can be aimed at in channel change convergence time.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the PLL circuit constituted from a conventional phase-comparison circuit mentioned above, there is a problem on which the reaction of a system becomes slow to the phase contrast near the dead zone.

[0017] For example, fR fP When the case where received and it becomes early for 12ns is assumed, it comes to be shown in drawing 7. In the state of the dead zone 0 of DZ = "0", it is an output Q1. Vt It can put at about 12ns and the time it is over is PD. Although "1" is outputted for 12ns as a signal a dead-zone 10ns [of DZ = "1"] state - output Q1 Vt about 2ns of time to exceed -- becoming -- PD As a signal, for 2ns continues but the rate of the integration voltage value change which controls VCO which lets a loop filter pass boils "1" dully.

[0018] If the property of this phase comparison is shown in drawing, it will become like drawing 8. fR fP Since the time which sees relatively and is deleted in 10ns for the dead-zone setup becomes small when phase contrast is large, although influence decreases, the sensitivity as a remarkable system deteriorates near the dead zone.

[0019] Specifically, although it is convenient to change to near shift frequency at the time of the change of the oscillation frequency of a PLL circuit, alignment near a convergence value is affected and there is a trouble which the phenomenon in which vibration drags on to a convergence value tends to produce.

[0020] The purpose of this invention is offering the PLL circuit which enabled stable synchronous convergence, preparing a dead zone at the time of a phase comparison.

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MEANS

[Means for Solving the Problem] They are the time constant circuit which is the PLL circuit which includes an armature-voltage-control oscillation means, a phase-comparison means make the phase comparison of this oscillation output-frequency signal and external oscillation signalling frequency, and a control-voltage generation means generate the control voltage of the aforementioned armature-voltage-control oscillation means according to this phase-comparison output according to this invention, and the aforementioned control-voltage generation means carries out as an input in a delay means to by which the aforementioned phase-comparison output is delayed, and the aforementioned phase-comparison output, and the output of the aforementioned delay means. When the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears, the PLL circuit characterized by being constituted including a latch means to cancel this latch state so that the aforementioned control voltage may be generated using this latch output is obtained.

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EXAMPLE

[Example] It explains in detail, referring to a drawing about the example of this invention below.

[0023] Drawing 1 is the block diagram of the example of this invention, and is reference frequency f_R . The output of generated VCO 1 turns into one input of a phase comparator 3. Frequency f_P which carried out dividing of the oscillation frequency of VCO7 to the other inputs of this phase comparator 3 with the counting-down circuit 2. The signal is impressed.

[0024] It is the lead signal PD of the pulse width according to the phase contrast from a phase comparator 3. It is behind, Signal PU is outputted and it is inputted into filter circuits 4a and 4b, respectively. These filter circuits 4a and 4b are circuits of the feature portion of this invention, and the one example is shown in drawing 2. They are PD and PU, a dead zone being set up in these filter circuits 4a and 4b. Phase contrast signals RU and RD with which pulse width (phase contrast information is included) does not change. It is generated.

[0025] These phase contrast signals RU and RD. It becomes the control voltage of VCO7 by being inputted into a loop filter 6 and finding the integral through the charge pump 5.

[0026] The output of this VCO7 serves as local oscillation frequency in a receiving system, change instructions of a receiving channel are answered, the oscillation frequency f_R of reference frequency VCO 1 and the division ratio of the program divider 2 are controlled, and the PLL frequency synthesizer is constituted.

[0027] Drawing 2 (A) and (B) are each example circuit diagram of the filter circuits 4a and 4b of drawing 1. First, if drawing 2 (A) is referred to, it is the lead signal PU. It is inputted into delay circuit 11a and time constant circuit 10a, respectively. The delay output of delay circuit 11a turns into a clocked into of D-FF13a which constitutes latch circuit 12a. [0028] The output of time constant circuit 10a turns into a base input of PNP transistor 15a which constitutes latch circuit 12a, and the emitter output of this transistor 15a turns into one input of OR-gate 14a while turning into a data input of D-FF13a. The delay output of delay circuit 11a is impressed to the other inputs of this OR-gate 14a, or the output is the reset input of D-FF13a. And the reversal Q output of D-FF13a is RU. It becomes.

[0029] Drawing 2 (B) is the delay signal PD. Although it consists of delay circuit 11b, time constant circuit 10b, and latch circuit 12b concretely also about the side. The polarity of the power supply line of time constant circuit 10b and the polarity of transistor 15b in a latch circuit progress, and it is Signal PU. It has become contrary to a side. Moreover, the collector output of transistor 15b is inverted in inverter 16b, and is the data input of D-FF13b, and one input of OR-gate 14b.

[0030] Drawing 3 is each signal wave form view showing operation of the circuit of drawing 2 (B), and is f_R . f_P When it receives and a phase is overdue, it is the delay signal PD. Two PDs from which it is a thing at the time of being outputted, and it is behind in this example, and a degree differs. The pulse is shown.

[0031] PD shown in (C). A pulse is changed into the loose wave (integration wave) of the standup shown in (d) with the time constant of time constant circuit 10b. This wave is the threshold V_t of transistor 15b. PD which is not attained. By the pulse, transistor 15b does not turn on and, therefore, the data input signal (D input signal) from inverter 16b to D-FF13b is not generated. On the other hand, an integration wave is Threshold V_t . PD to attain. By the pulse, transistor 15b is generated, as it turns on and a data input signal shows (e) from inverter 16b, and for this data input signal, an integration wave is Threshold V_t . It is generated until it becomes smallness.

[0032] the clocked into of D-FF13b -- PD a pulse -- time t_D only -- **** delay PD shown in delayed (f). The pulse is supplied. Here, it is a time delay t_D . Same [in the time t_M (refer to drawing (e)) to become settled with the time constant of time constant circuit 10b / almost] or it is t_M . t_D If it selects to smallness a little, it synchronizes with the standup timing of a clock signal (delay pulse PD), and a data input signal is incorporated and latched to D-FF13b.

[0033] Delay PD. It is the filter circuit output RD which a latch state is reset and is shown in (g) as a result since D-FF13b will be reset by the output of OR-gate 14b, if a pulse falls. It will be obtained.

[0034] Therefore, lead signal PD according to phase contrast. Therefore, it is the threshold V_t of filter circuit 12b, without being inputted into the latter charge pump 5 by letting filter circuit 4b (drawing 1) pass depending on the degree of the phase contrast. Time t_M to become settled. It becomes a dead zone.

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[0037] Stopping at the circuit of drawing 2 only being shown in an example, it is clear for various circuit deformation to be
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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of the PLL circuit by this invention.

[Drawing 2] It is the circuit diagram showing an example of the filter circuits 4a and 4b of drawing 1.

[Drawing 3] It is each part operation wave form chart of the circuit of drawing 2.

[Drawing 4] It is the phase-comparison property view of the PLL circuit by this invention.

[Drawing 5] It is the circuit diagram of the phase comparator of the conventional PLL circuit.

[Drawing 6] It is each wave form chart of the circuit of drawing 5 of operation.

[Drawing 7] It is each wave form chart of the circuit of drawing 5 of operation.

[Drawing 8] It is the phase-comparison property view of the circuit of drawing 5.

[Description of Notations]

1 Reference Frequency VCO

2 Counting-down Circuit

3 Phase Comparator

4a, 4b Filter circuit

5 Charge Pump

6 Loop Filter

7 VCO

10a, 10b Time constant circuit

11a, 11b Delay circuit

12a, 12b Latch circuit

13a, 13b D-FF

14a, 14b OR gate

15a, 15b Transistor

16b Inverter

[Translation done.]

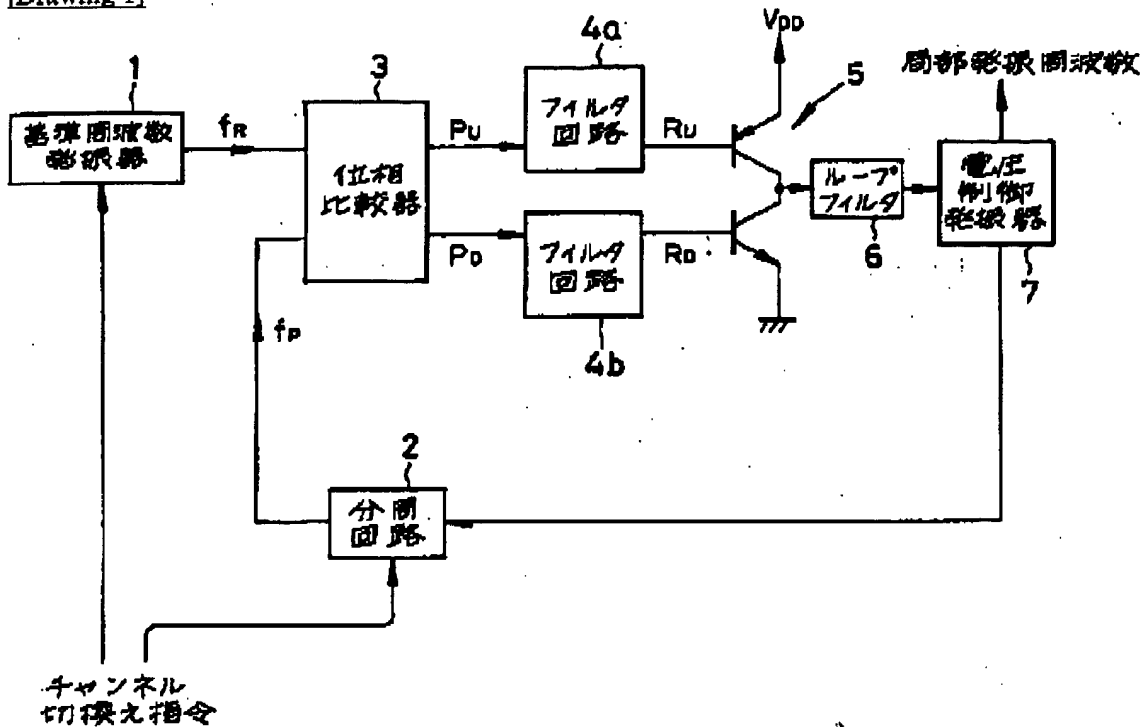
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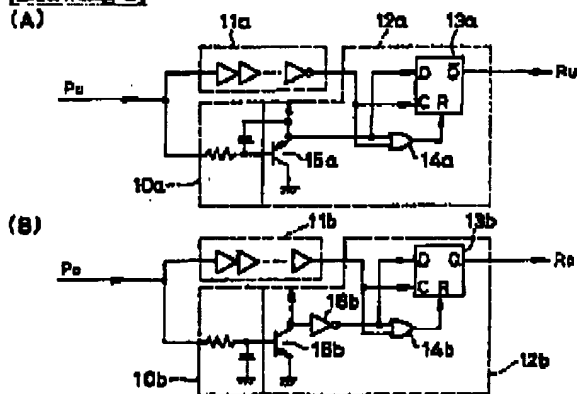
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DRAWINGS

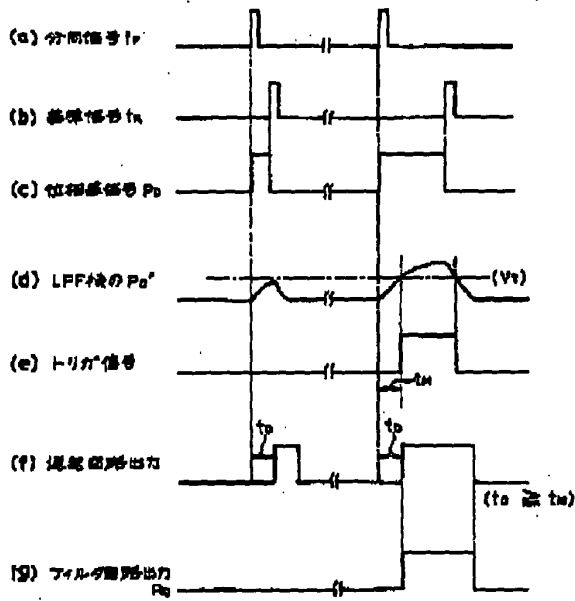
[Drawing 1]



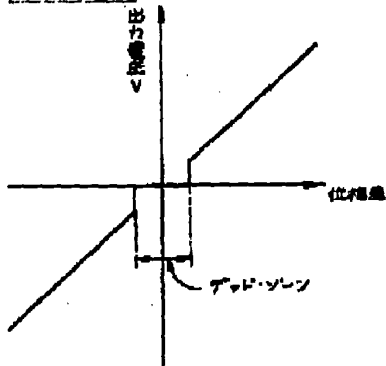
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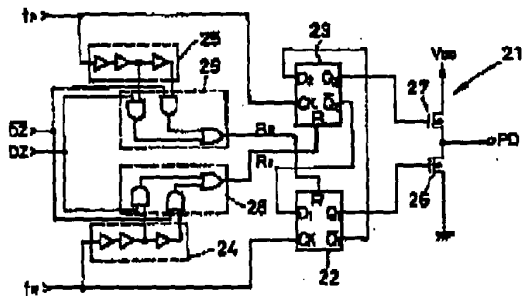
[Drawing 3]



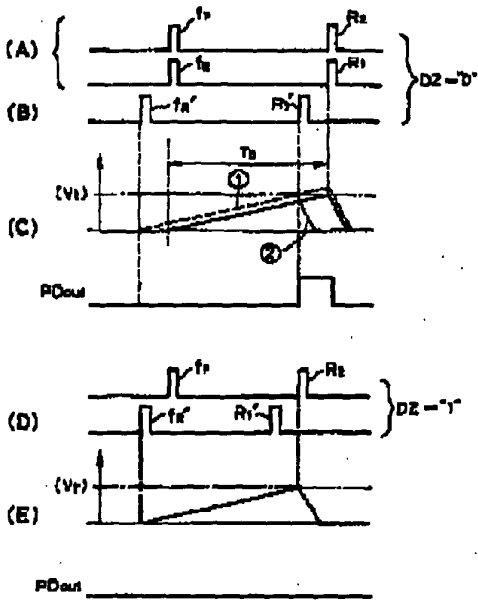
[Drawing 4]



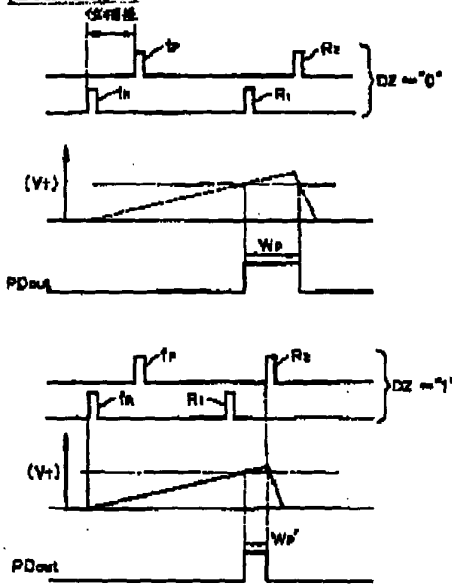
[Drawing 5]



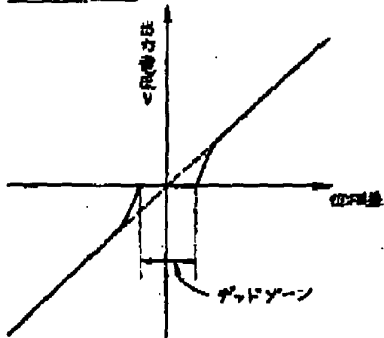
[Drawing 6]



[Drawing 7]



[Drawing 8]



[Translation done.]